CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1-5. (Cancelled)

6. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a plurality of client computers, wherein each client computer of said plurality generates a test job for testing a different design of a programmable logic circuit and comprises test vectors and configuration data for said different design of a programmable logic circuit;

a server coupled to said plurality of client computers ~~by way of~~ through a network interface, said server receiving a predetermined test job from a ~~predetermined~~ client computer; and

a plurality of systems under test coupled to said server and shared among said plurality of client computers ~~by way~~ through said network interface under the control of said server, wherein each system under test of said plurality of systems under test has a different programmable logic device architecture, and wherein each system under test of said plurality of systems under test has a programmable logic circuit which is configured with said design of a programmable logic circuit implemented according to configuration data of said predetermined test job from said ~~predetermined~~ client computer ~~by way~~ through said network interface of said server and receives corresponding test vectors of said predetermined test job of said ~~predetermined~~ client computer and outputs result vectors to said ~~predetermined~~ client computer ~~by way~~ through said network interface of said server.

7. (Cancelled)

8. (Original) The system of claim 6 wherein said server comprises a system under test interface.

9. (Cancelled)

10. (Currently Amended) The system of claim 6 further comprising another server coupled to said plurality of client computers ~~by way of the network~~ through said network interface.

11. (Withdrawn) A client-server semiconductor verification system, said system comprising:

a plurality of client computers, wherein each client computer of said plurality generates a test job for testing a different design of a programmable logic circuit and has test vectors and configuration data for said different design of a programmable logic circuit;

a job distribution server coupled to said plurality of client computers by way of a network, said job distribution server receiving a test job from a predetermined client computer;

a server coupled to said plurality of client computers by way of said job distribution server, said server receiving said test job from said predetermined client computer by way of said job distribution server; and

a plurality of systems under test having different programmable logic device architectures and shared among the plurality of client computers, each system under test having programmable logic which is configured with a design of a programmable logic circuit according to configuration data of said test job from said predetermined client computer and coupled to each system under test by way of said server, wherein each system under test receives corresponding test vectors and outputs result vectors to said predetermined client computer by way of said server and said job distribution server.

12. (Withdrawn) The system of claim 11 further comprising a plurality of

servers coupled to said plurality of client computers by way of said job distribution server.

13. (Withdrawn) The system of claim 12 wherein said plurality of servers are coupled to said job distribution server by way of a second network.

14-20. (Cancelled)

21. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client computers to a test server, each said client computer storing a test job for testing a different design of a programmable logic circuit, each test job having test vectors and configuration data for said different design of a programmable logic circuit;

providing a plurality of systems under test, each system under test having a different programmable logic device architecture and shared among the plurality of client computers through a network interface under the control of a test server;

reconfiguring a programmable logic circuit of each system under test with a design of a programmable logic circuit stored in a ~~predetermined~~ client computer according to configuration data of a predetermined test job ~~by way of a~~ through said network interface of said test server;

coupling corresponding test vectors of said predetermined test job for said design of a programmable logic circuit from said ~~predetermined~~ client computer to each system under test ~~by way~~ through said network interface of said test server;

receiving an output comprising result vectors from each system under test; and

comparing said result vectors from each system under test to expected result vectors.

22. (Previously Presented) The method of claim 21 further comprising a

step of coupling said plurality of systems under test to said test server.

23. (Currently Amended) The method of claim 21 further comprising a step of providing a test server having ~~a network interface and~~ a system under test interface.

24. (Currently Amended) The method of claim 23 further comprising a step of coupling said result vectors to said ~~predetermined~~ client computer ~~by way~~ through said network interface of said test server.

25. (Currently Amended) The method of claim 21 wherein said step of comparing said result vectors from each system under test to expected result vectors comprises comparing said result vectors from each system under test to expected result vectors at said ~~predetermined~~ client computer.

26. (Withdrawn) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client computers to a job distribution server, each said client computer storing a test job for testing a different design of a programmable logic circuit and having test vectors and configuration data for said different design of a programmable logic circuit;

providing a plurality of systems under test, each system under test having a different programmable logic device architecture and shared among the plurality of client computers;

reconfiguring a programmable logic circuit of each system under test of said plurality of systems under test with a design of a programmable logic circuit according to configuration data of a test job stored in a predetermined client computer and received at each system under test by way of a job distribution server;

coupling said job distribution server to a plurality of servers, each said server coupling predetermined test vectors to a system under test of said plurality of systems under test;

receiving an output comprising result vectors from each system under

test of said plurality of systems under test; and

comparing said result vectors from each system under test to expected result vectors.

27. (Withdrawn) The method of claim 26 further comprising a step of providing a first network between said plurality of client computers and said job distribution server.

28. (Withdrawn) The method of claim 27 further comprising a step of providing a second network between said plurality of servers and said job distribution server.

29. (Withdrawn) The method of claim 26 further comprising coupling said plurality of systems under test to a server of said plurality of servers.

30. (Withdrawn) The method of claim 26 further comprising a step of coupling said output comprising result vectors to a client computer.